Variability Study for Low-Voltage Microelectromechanical Relay Operation

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***Abstract*— Body-biased microelectromechanical relays previously have been developed for ultralow-power digital logic applications and demonstrated to reliably switch ON/OFF with sub-50-mV gate voltage swing. Since variability in relay switching voltages can practically limit reduction in the operating voltage of a relay-based integrated circuit, the effects of process-induced variations and device operating conditions, as well as the stability of relay switching voltages, are investigated in this paper. Antistiction coating is shown to stably reduce hysteresis voltage and random variation thereof, which is beneficial for voltage scaling.**

***Index Terms*— Antistiction, body bias, microelectromechanical (MEM) relay, molecular coating, perfluorooctyltriethoxysilane (PFOTES), process-induced variation, switching stability, variability.**

I. Introduction

FOR decades, the growth of the semiconductor industry has been enabled by the steady miniaturization of semiconductor-based switches, predominantly MOSFETs, in accordance with Moore's Law. In recent years, however, the incremental benefits of transistor scaling have been diminished due to nonideal switching behavior—in particular, nonzero leakage current (I_{OFF}) and temperature-dependent nonzero subthreshold swing (SS)—limiting the extent to which the transistor threshold voltage and hence the IC operating voltage (V_{DD}) can be lowered beneficially [1]. Therefore, there have been many efforts to develop alternative solid-state switch designs that can achieve more ideal (i.e., abrupt) switching characteristics [2]–[4].

Although experimental transistor designs such as the tunnel field-effect transistor (TFET) [2] and negative capacitance FET (NC-FET) [3] can achieve steeper switching characteristics than the MOSFET, they also can be more sensitive to process-induced variations and device operating conditions which practically limit their benefits. For example, switching abruptness can be degraded by trap-assisted tunneling due to interfacial defects in a TFET [5] and by polarization screening in an NC-FET [6].

Microelectromechanical (MEM) switches can achieve immeasurably low I_{OFF} and abrupt switching behavior across a wide range of temperatures [7]; in principle, they can be operated with much lower voltage than can any type of transistor. (Although they switch more slowly than do transistors, circuit design optimization to minimize the number of mechanical switching delays per function can compensate for this [8].) Thus, MEM switches are of keen interest for digital IC applications for which energy efficiency is paramount, such as wirelessly networked devices in the emerging Internet of Things.

A body-biased MEM relay design was previously developed for digital IC applications [9] and shown to provide for the most energy efficient operation [10]. With antistiction coating to reduce the hysteresis voltage (V_H), relay operation with sub-50-mV gate voltage (V_G) swing has been demonstrated [11]. However, variability in relay switching voltages (namely, the pull-in voltage V_{PI} and the release voltage V_{RL}, $V_H \equiv |V_{PI} - V_{RL}|$) can practically limit reductions in operating voltage. Therefore, the effects of process-induced variations and device operating conditions, as well as the stability of relay switching voltages, are investigated in this paper. A nonzero strain gradient within the structural layer is found to mitigate the effect of systematic variation in layer thickness, but to result in significant random variation, which is identified to

Manuscript received November 10, 2017; revised January 26, 2018; accepted February 12, 2018. Date of publication February 27, 2018; date of current version March 22, 2018. This work was supported by the Center for Energy Efficient Electronics Science, National Science Foundation (NSF) under Award 0939514. The work of B. Osoba was supported by NSF. The review of this paper was arranged by Editor F. Ayazi. *(Corresponding author: Benjamin Osoba.)*

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Digital Object Identifier 10.1109/TED.2018.2807409

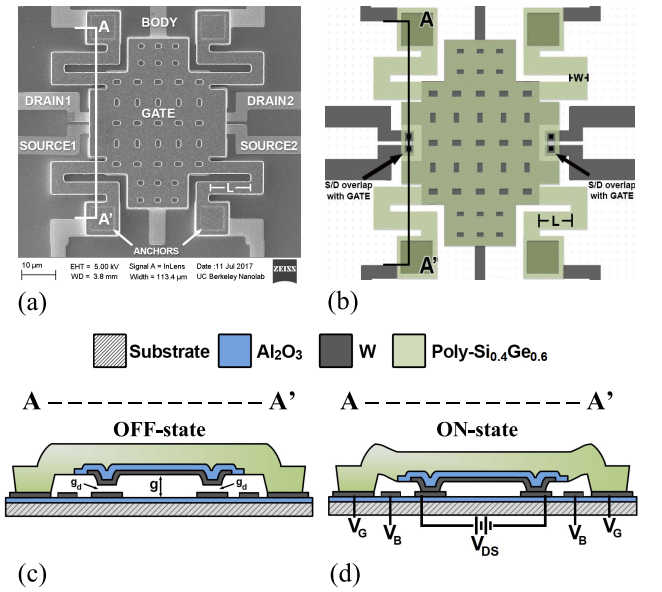

Fig. 1. Plan view (a) scanning electron micrograph and (b) mask layout of the six-terminal relay design used in this paper. The flexural beam length L and width W are indicated. The cross section A–A' is shown in (c) OFF-state and (d) ON-state. In the ON-state, surface adhesive force is introduced resulting in hysteresis.

TABLE I
NOMINAL DESIGN PARAMETER VALUES FOR RELAYS USED IN THIS PAPER

Design Parameter	Value
Poly-$Si_{0.4}Ge_{0.6}$ Thickness, t	1.6 μm
Beam Width, W	2 μm
Beam Length, L	{8, 12} μm
Actuation Area, A	1236 μm^2
Actuation Gap, g	220 nm
Contact Dimple Gap, g_d	60 nm
Contact Area, A_{CONT}	1 μm^2

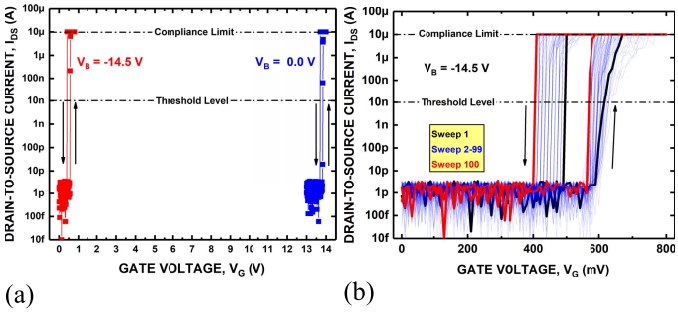

Fig. 2. (a) Measured I–V characteristics for a relay operated at $V_{DS} = 1$ V and various body bias voltages V_B. (b) Stable low-voltage operation is enabled by body biasing, with less than 100-mV variation in V_{PI} and V_{RL} over 100 gate voltage sweeps. V_{PI} and V_{RL} are taken to be the corresponding voltages at which I_{DS} crosses the threshold level, 10 nA. The ON-state current was artificially limited to 10 μA, to prevent excessive Joule heating resulting in microwelding. $L = 8$ μm.

be the primary limiter of V_{DD} scaling for relay-based circuits. More specifically, such strain gradient causes out-of-plane deflection upon release, in turn affecting the actuation gap size g; because this out-of-plane deflection is reduced for thicker structural layers, the effects on V_{PI} for stiffer structures are reduced [12]. Antistiction coating is found to be effective for stably reducing V_H magnitude and random variation, to facilitate V_{DD} reduction.

II. Relay Structure and Operation

The six-terminal relay design [13] used in this paper includes a movable gate electrode suspended by four folded-flexure suspension beams over a fixed body electrode on an insulating substrate, as shown in Fig. 1. Narrow conductive strips are attached underneath the movable electrode (but electrically insulated from it by an intermediary layer of Al_2O_3), so that each of them comes into contact with a pair of source and drain electrodes—allowing current to flow between source and drain—when a sufficiently large voltage is applied between the gate and body to electrostatically actuate the movable electrode downward.

The relay fabrication process flow is described in [13]. The structural material (used for the gate electrode and suspension beams) is polycrystalline silicon germanium (poly-$Si_{0.4}Ge_{0.6}$) deposited by low-pressure chemical vapor deposition (LPCVD) at 410 °C; the fixed electrode material (used for gate–source–drain electrodes) is tungsten (W) deposited by sputtering; the substrate and channel insulating layers of Al_2O_3 were deposited by atomic layer deposition (ALD) at 300 °C and plasma-enhanced ALD at 250 °C, respectively. The air gaps in the actuation region and contact regions were formed by selectively removing sacrificial layers of SiO_2 (deposited by LPCVD at 400 °C), to "release" the structure for movement. Nominal film and air gap thicknesses are listed in Table I.

Note that the relays were designed to operate in nonpull-in mode (i.e., the nominal contact gap size g_d is less than one-third the nominal actuation gap size g) to minimize hysteretic switching behavior. However, due to nonzero strain gradient in the poly-$Si_{0.4}Ge_{0.6}$ [12] causing out-of-plane deflection upon release (substantially increasing both g_d and g), the relays in this paper actually operate in pull-in mode (and hence have larger hysteresis voltage), so that the switching voltages are given by the following equations:

$$V_{PI} = \sqrt{\frac{8k_{\text{eff}}g^3}{27\varepsilon_0 A}} \tag{1}$$

$$V_{RL} = \sqrt{\frac{2(k_{\text{eff}}g_d - F_A)(g - g_d)^2}{\varepsilon_0 A}} \tag{2}$$

where k_{eff} is the effective spring constant, ε_0 is the vacuum permittivity, A is the effective actuation area, and F_A is the contact adhesive force.

III. Experimental Results

The relays in this paper were tested at room temperature under vacuum (~1.5 μTorr). Fig. 2 shows typical dc measurements (forward and backward V_G sweeps, monitoring drain-to-source current) of relay switching behavior. As explained

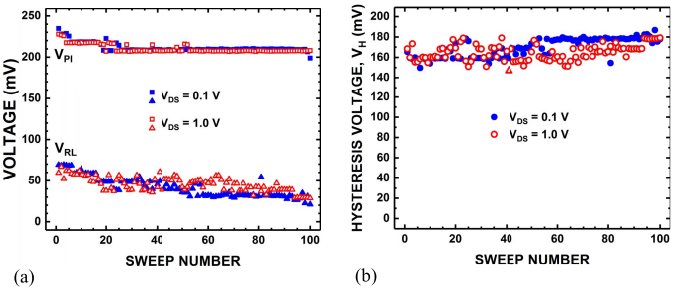

Fig. 3. Evolution of (a) relay switching voltages and (b) V_H for relay operated at $V_B = -14.5$ V and various values of drain-to-source voltage V_{DS}. The current compliance limit was set to 10 μA. $L = 8$ μm.

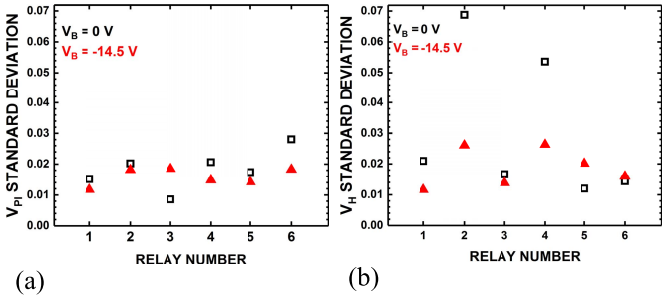

Fig. 4. Measured variability in (a) V_{PI} and (b) V_H for multiple relays operated at $V_{DS} = 1$ V with $V_B = 0$ V or $V_B = -14.5$ V. Body biasing generally decreases variability in V_{PI} and V_H. The current compliance limit was set to 10 μA. $L = 8$ μm.

in [10], high device manufacturing yield can be achieved by designing relays to have relatively stiff structures and large air gaps as fabricated; subsequently they can be made to operate with a small V_G swing by applying a bias voltage (V_B) to the body. [Note: The shift in gate switching voltage is slightly smaller than the magnitude of the body-bias voltage because the body electrode has slightly smaller area than does the gate electrode, as can be seen from Fig. 1(a).]

The minimum operating voltage of a relay is equal to the minimum V_G swing required to switch the device ON/OFF, which cannot be smaller than V_H. For a circuit comprising many devices, V_{DD} scaling is constrained by the maximum and minimum values of V_{PI} and V_{RL}, respectively. Process-induced variations in relay dimensions, as well as random variations in F_A from device to device and over the device operating lifetime, result in switching voltage variations discussed in Section III-B.

A. Relay Switching Voltage Stability

Fig. 3 shows measured switching voltages for 100 sequential dc measurements made on a single body-biased relay. It should be noted that this switching operation is much more stressful than operation within a digital IC where a relay would only sustain a significant voltage drop across the source and drain electrodes and conduct current for very short periods of time corresponding to the RC charging delay (~1 ps) [8]. V_{PI} is very stable after the first ~20 sweeps. V_H varies slightly (by ~20 mV), likely due to variation in actual contact area for each switching cycle. Weak dependence on the drain-to-source voltage (V_{DS}) is seen.

Fig. 4 shows that body biasing is generally advantageous for improving switching voltage stability (i.e., reducing variability in V_{PI} and V_H).

B. Process-Induced Variations

The LPCVD processes used to deposit the SiO_2 and poly-$Si_{0.4}Ge_{0.6}$ layers in this paper resulted in significant systematic variations across a wafer (i.e., die–die) and random variations from device to device, in the thicknesses of the actuation and contact gaps and the movable structure, as determined using an Olympus LEXT OLS4000 3D confocal laser microscope.

Fig. 5(a) shows how V_{PI} varies with poly-$Si_{0.4}Ge_{0.6}$ thickness. Utilizing (1) and noting that $k_{eff} \propto t^3$, the theoretical relationship between poly-$Si_{0.4}Ge_{0.6}$ thickness t, actuation gap g, and V_{PI} is as follows:

$$V_{PI} = \left(\frac{g * t}{g_0 * t_0}\right)^{3/2} * V_{PI_0}. \tag{3}$$

By comparing the measured V_{PI} values against the theoretically predicted trend based on (3), taking into account the negative correlation between structural layer thickness and actuation gap size as shown in Fig. 5(b), it can be seen that random sources of variation are predominant. (Measured values $g_0 = 0.35$ μm, $t_0 = 1.5$ μm, and $V_{PI_0} = 11.9$ V were used to calibrate the theoretical curve.) The systematic variation is relatively small and can be further reduced in a relatively straightforward manner with an improved LPCVD process control. Fig. 5(c) shows that there is a significant random variation in V_H, which depends on local contact properties that vary from device to device. Switching voltage variations practically limit the extent to which V_{DD} can be reduced: in practice, a single negative value of V_B should be used for all of the "pull-down" relays within a circuit block, while another single positive value of V_B should be used for all of the "pull-up" relays within a circuit block; to guarantee that every relay is functional, $|V_B|$ can be no larger than the smallest $|V_{RL}|$.

Fig. 6 shows the variation in switching voltages for relays located side by side on a single die, with the same value of V_B that was chosen to guarantee circuit functionality. Although V_H can be less than 100 mV, random variability limits V_{DD} to be not less than ~0.9 V for this die. More uniform (device–device) switching voltages are necessary to overcome this issue, to fully realize the benefit of relay technology for ultralow-voltage ICs.

C. Effects of Antistiction Coating

In prior work, we demonstrated that a hydrophobic coating of perfluorodecyltriethoxysilane (PFDTES) is effective for reducing V_H, but at a tradeoff of increased SS, i.e., less abrupt switching behavior [11]. As seen in Fig. 7, a molecular coating with a shorter perfluoro chain, perfluorooctyltriethoxysilane (PFOTES), was used in this paper to mitigate the aforementioned tradeoff.

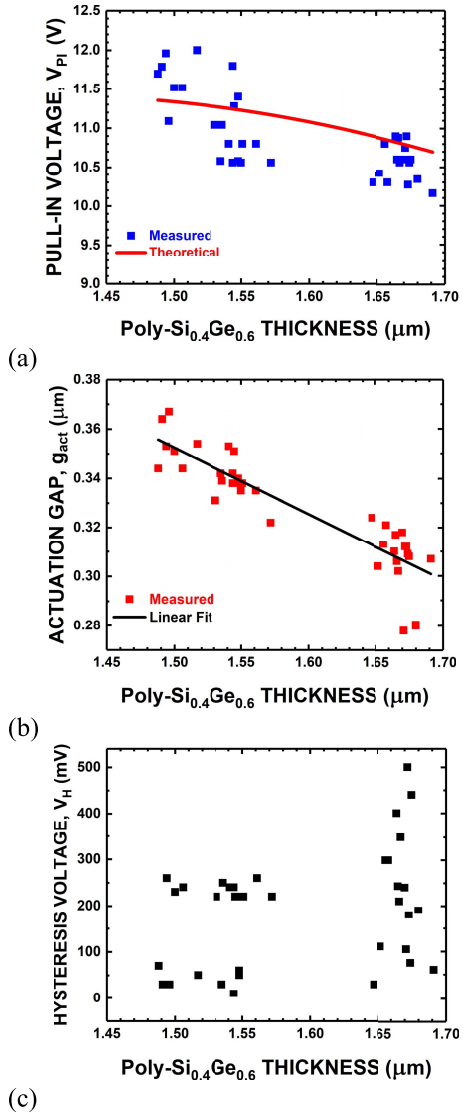

Fig. 5. Measured impact of process-induced variations in poly-$Si_{0.4}Ge_{0.6}$ thickness on (a) V_{PI} for relay operated at $V_B = 0$ V, (b) actuation gap g, and (c) hysteresis voltage V_H. The negative correlation between the structural layer thickness and actuation gap size is due to the reduced out-of-plane deflection for a stiffer structure. $L = 12$ μm.

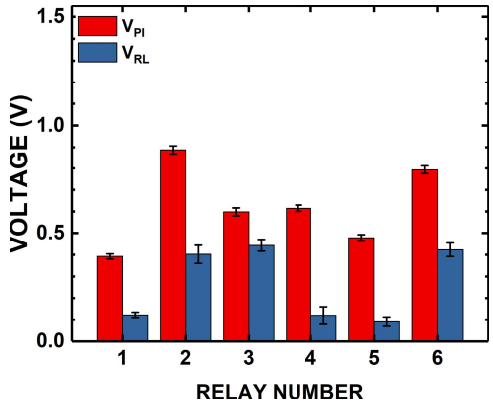

Fig. 6. Measured switching voltages for multiple relays operated at $V_{DS} = 1$ V, $V_B = -14.5$ V. $L = 8$ μm.

As can be seen from Fig. 8, a PFOTES-coated relay can be fully switched between ON and OFF states with sub-50-mV V_G swing.

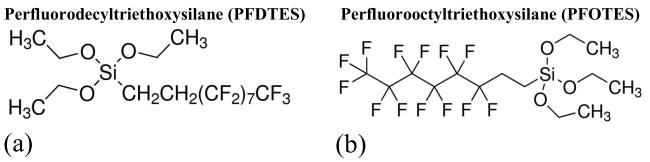

Fig. 7. Molecular structure of (a) PFDTES versus (b) PFOTES.

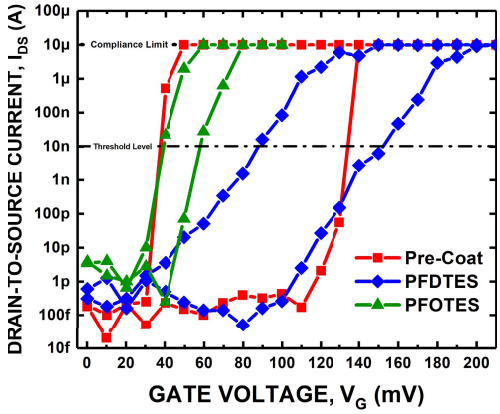

Fig. 8. Measured I–V characteristics for body-biased relays, showing the effects of antistiction coatings. $L = 12$ μm.

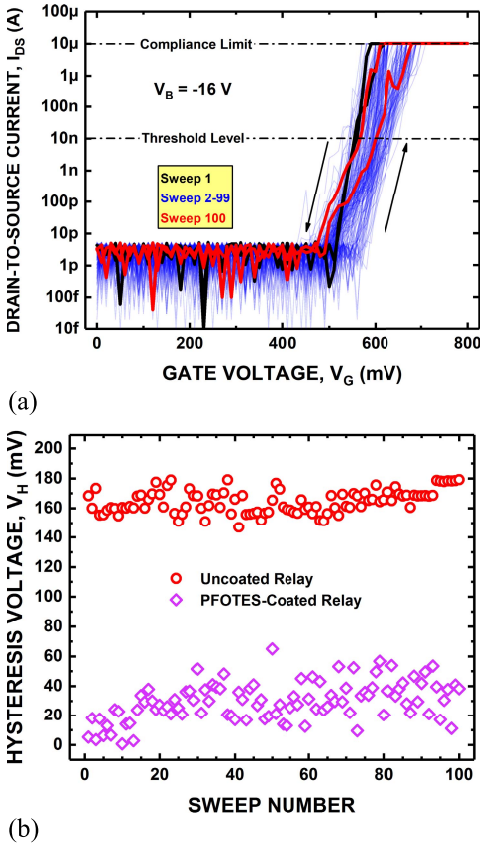

Fig. 9. (a) Measured I–V characteristics. (b) Evolution of measured V_H for PFOTES-coated MEM relay operated over 100 gate voltage sweeps at $V_{DS} = 1$ V and body-biased conditions. These data indicate significantly decreased value and variability in V_H due to the PFOTES coating. $L = 8$ μm.

Fig. 9 shows that low V_H is stably maintained with PFOTES coating over many switching cycles.

The data in Fig. 10(a) affirm that relay switching stability is improved with the antistiction coating. Fig. 9(b) shows that

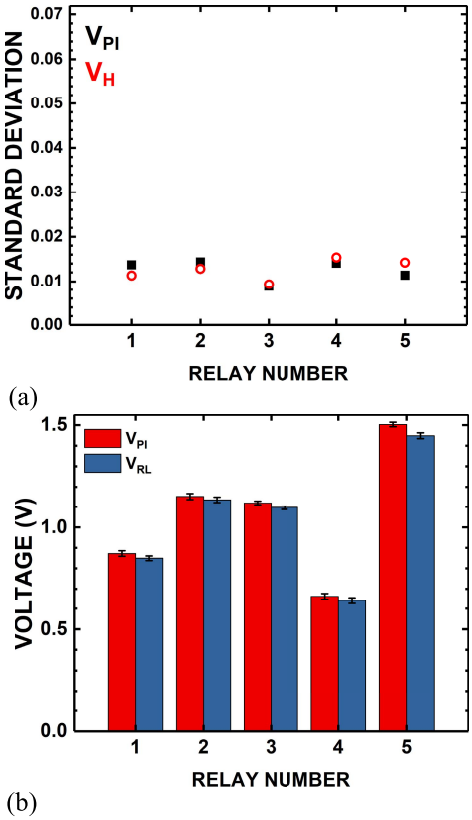

Fig. 10. Measured (a) variability in V_{PI} and V_H and (b) switching voltages for multiple PFOTES relays operated at $V_{DS} = 1$ V and $V_B = -16$ V. $L = 8$ μm.

device to device variation in V_H is also significantly improved, indicative of more uniform contact properties for the coated relays.

IV. Discussion

The results of this paper indicate that variation in V_{PI} will practically limit V_{DD} reduction for relay-based ICs. Because the microstructure of the LPCVD poly-$Si_{0.4}Ge_{0.6}$ structural film is highly nonuniform [12], out-of-plane deflection due to nonzero strain gradient is significant and varies from device to device, resulting in large random variation in V_{PI} as seen in Fig. 5. This issue can be mitigated using a much thicker (stiffer) poly-$Si_{0.4}Ge_{0.6}$ film, but at a tradeoff of a much larger gate-to-body voltage required to turn ON the relay, i.e., larger $|V_B|$. Alternatively, a structural film with zero strain gradient could be developed. For instance, multitarget dc magnetron sputtering has been demonstrated to effectively and controllably grow amorphous metal thin films [14], [15].

V. Conclusion

The effects of process-induced variations, device operating conditions, and antistiction coating on the variability and stability of MEM relay switching voltages were studied in this paper. Tight control ($\pm 1\%$) of the structural layer thickness and the actuation and contact gap thicknesses are necessary to enable sub-100-mV relay-based circuit operation. In this regard, a structural layer material with low residual stress and an amorphous microstructure may be necessary to minimize random out-of-plane deflection. An optimized antistiction coating is effective for reducing hysteresis and random variation thereof, and hence, is expected to facilitate the practical implementation of sub-100-mV relay-based circuits. Furthermore, variation in V_{PI} is reduced with the antistiction molecular coating.

Acknowledgment

The microelectromechanical relays were fabricated in the Marvell Nanofabrication Laboratory at the University of California at Berkeley, Berkeley, CA, USA.

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